WHAT IS CLAIMED IS:

1. A method of processing data packets comprising:

generating an enqueue command specifying a queue descriptor associated with a new buffer in response to receiving an enqueue request, with the queue descriptor stored in a cache and the queue descriptor having a head pointer pointing to a first buffer in a queue of buffers and a tail pointer pointing to a last buffer in the queue of buffers and with the first buffer having a buffer pointer pointing to a next buffer in the queue;

setting a buffer pointer associated with the last buffer to point to the new buffer; and

setting the tail pointer to point to the new buffer.

2. The method of claim 1 further comprising:

setting the tail pointer to point to another buffer in response to receiving an enqueue request with respect to said other buffer.

3. The method of claim 1 further comprising:

generating a dequeue command specifying the queue descriptor associated with the first buffer in response to receiving a dequeue request with respect to the first buffer, and setting the head pointer to point to the next buffer.

4. The method of claim 3 further comprising:

setting the head pointer to point to a buffer pointed to by the next buffer in response to receiving a dequeue request with respect to the next buffer.

5. The method of claim 1 comprising:

replacing a queue descriptor with the queue descriptor associated with the new buffer, if the queue descriptor associated with the new buffer is not in the cache.

6. An apparatus for processing data packets comprising:

a first memory comprising:

a queue of buffers, having a first buffer with a buffer pointer pointing to a next buffer in the queue, and

a cache of queue descriptors, each of which has a head pointer pointing to the first buffer in the queue, and a tail pointer pointing to a last buffer in the queue;

a processor coupled to the first memory; and

a computer-readable medium storing instructions that when applied to the processor, cause the processor to:

generate an enqueue command specifying a queue descriptor associated with a new buffer, in response to

receiving an enqueue request associated with the new buffer,

set a buffer pointer associated with the last buffer to point to the new buffer, and

set the tail pointer to point to the new buffer.

7. The apparatus of claim 6 wherein the processor is configured to:

set the tail pointer to point to the other buffer, in response to receiving an enqueue request with respect to another buffer.

8. The apparatus of claim 6 wherein the processor is further configured to:

generate a dequeue command specifying a queue descriptor associated with the first buffer and set the head pointer to point the next buffer in response to receiving a dequeue request with respect to the first buffer.

9. The apparatus of claim 8 wherein the processor is configured to:

set the head pointer to point to a buffer pointed to by the next buffer in response to receiving a dequeue request with respect to the next buffer.

10. The apparatus of claim 6 wherein the processor is configured to:

replace a queue descriptor with the queue descriptor associated with the new buffer, if the queue descriptor associated with the new buffer is not in the cache.

11. The apparatus of claim 10 wherein the processor is further configured to replace a queue descriptor based on a least recently used (LRU) policy.

12. The apparatus of claim 6 wherein each buffer in the queue includes pointers to data buffers having data packets residing in a second memory.

13. The apparatus of claim 6 wherein the cache of queue descriptors includes approximately 16 queue descriptors.

14. The apparatus of claim 6 wherein each buffer in the queue includes a count field having a value representing the number of buffers in the queue.

15. The apparatus of claim 6 wherein the queue is a linked list of buffers.

16. An article comprising a computer-readable medium that stores computer executable instructions for causing a computer system to:

generate an enqueue command specifying a queue descriptor associated with the new buffer in response to receiving an enqueue request, the queue descriptor being stored in a cache of queue descriptors, the queue descriptors having a head pointer pointing to a first buffer in a queue and a tail pointer pointing to a last buffer in the queue, the first buffer having a buffer pointer pointing to a next buffer in the queue;

set a buffer pointer associated with the last buffer to point to the new buffer; and

set the tail pointer to point to the new buffer.

17. The article of claim 16, including instructions for causing the computer to:

set the tail pointer to point to the other buffer in response to receiving an enqueue request with respect to another buffer.

18. The article of claim 16, including instructions for causing the computer to:

generate a dequeue command specifying the queue descriptor associated with the first buffer and set the head pointer to point to the next buffer, in response to receiving a dequeue request with respect to the first buffer.

19. The article of claim 18, including instructions for causing the computer to:

set the head pointer to point to a buffer pointed to by the next buffer, in response to receiving a dequeue request with respect to the next buffer.

20. The article of claim 16, including instructions for causing the computer to:

replace a queue descriptor with the queue descriptor associated with the new buffer, if the queue descriptor associated with the new buffer is not in the cache.

21. A system comprising:

a source of data packets grouped into data buffers;

a destination for the data buffers; and

an apparatus coupled to the source of the data packets and to the destination of the data buffers, the apparatus comprising:

a first memory comprising:

a queue of buffers having a first buffer with a buffer pointer pointing to a next buffer in the queue, and

a cache of queue descriptors, each of which has a head pointer pointing to the first buffer in the

queue and a tail pointer pointing to a last buffer in the queue, and

a processor coupled to the first memory, and

a computer-readable medium storing instructions that when applied to the processor, cause the processor to:

generate an enqueue command specifying a queue descriptor associated with a new buffer,

set a buffer pointer associated with the last buffer to point to the new buffer, and

set the tail pointer to point to the new buffer.

22. The system of claim 21 wherein the processor is further configured to:

set the tail pointer to point to the other buffer, in response to receiving an enqueue request with respect to another buffer.

23. The system of claim 21 wherein the processor is further configured to:

generate a dequeue command specifying a queue descriptor associated with the first buffer and set the head pointer to point to the next buffer, in response to receiving a dequeue request with respect to the first buffer.

24. The system of claim 23 wherein the processor configured to:

set the head pointer to point to a buffer pointed to by the new buffer, in response to receiving a dequeue request with respect to the new buffer.

25. The system of claim 21 wherein the processor is configured to:

replace a queue descriptor with the queue descriptor associated with the next buffer, if the queue descriptor associated with the next buffer is not in the cache.

26. The system of claim 21 wherein the processor is further configured to replace a queue descriptor based on a least recently used (LRU) policy.

27. The system of claim 21 wherein each buffer in the queue includes pointers to data buffers containing data packets residing in a second memory.

28. The system of claim 21 wherein the cache of queue descriptors includes approximately 16 queue descriptors.

29. The system of claim 21 wherein each buffer in the queue includes a count field having a value representing the number of buffers in the queue.

30. The system of claim 21 wherein the queue is a linked list of buffers.